512 Kbit (x8) Multi-Purpose Flash
SST39SF512

Data Sheet

FEATURES:

- **Organized as 64K x8**
- **Single 4.5-5.5V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption (typical values at 14 MHz)**
  - Active Current: 10 mA (typical)
  - Standby Current: 10 µA (typical)
- **Sector-Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 70 ns
- **Latched Address and Data**
- **Fast Erase and Byte-Program**
  - Sector-Erase Time: 7 ms (typical)
  - Chip-Erase Time: 15 ms (typical)
  - Byte-Program Time: 20 µs (typical)
  - Chip Rewrite Time: 2 seconds (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **TTL I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
  - 32-pin PDIP

PRODUCT DESCRIPTION

The SST39SF512 are CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39SF512 devices write (Program or Erase) with a 4.5-5.5V power supply. The SST39SF512 device conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance Byte-Program, the SST39SF512 devices provide a maximum Byte-Program time of 30 µsec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39SF512 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39SF512 are offered in 32-lead PLCC, 32-lead TSOP, and a 600 mil, 32-pin PDIP packages. See Figures 1, 2, and 3 for pin assignments.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39SF512 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 4).

Byte-Program Operation

The SST39SF512 are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 30 µs. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 15 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 9 for timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Chip-Erase Operation

The SST39SF512 provide Chip-Erase operation, which allows the user to erase the entire memory array to the “1s” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 10 for timing diagram, and Figure 18 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST39SF512 provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the Program or Erase cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST39SF512 are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even thought DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program Operation. For sector or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0s and 1s, i.e., toggling between 0 and 1. The Toggle Bit will begin with "1". When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 16 for a flowchart.

Data Protection

The SST39SF512 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39SF512 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte load sequence. The SST39SF512 device is shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC}.

Product Identification

The Product Identification mode identifies the device as the SST39SF512 and SST39SF010 and manufacturer as SST. This mode may be accessed by software operations. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, Table 4 for software operation, Figure 11 for the software ID entry and read timing diagram and Figure 17 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

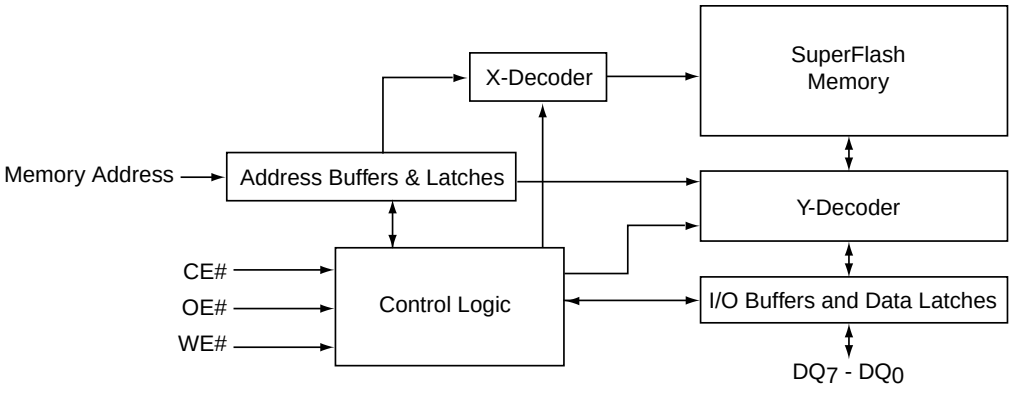
	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST39SF512	0001H	B4H

T1.3 1149

Product Identification Mode Exit/Reset

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform and Figure 17 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM



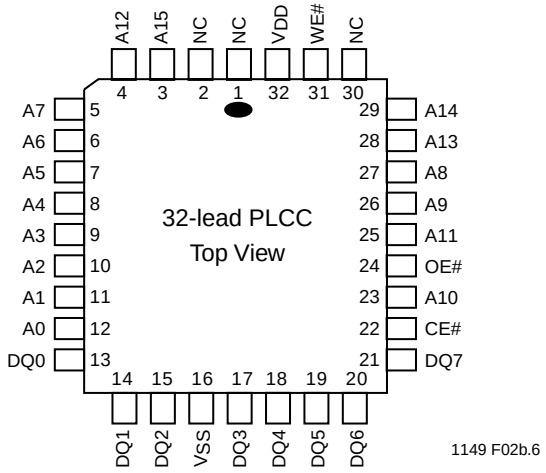


FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC

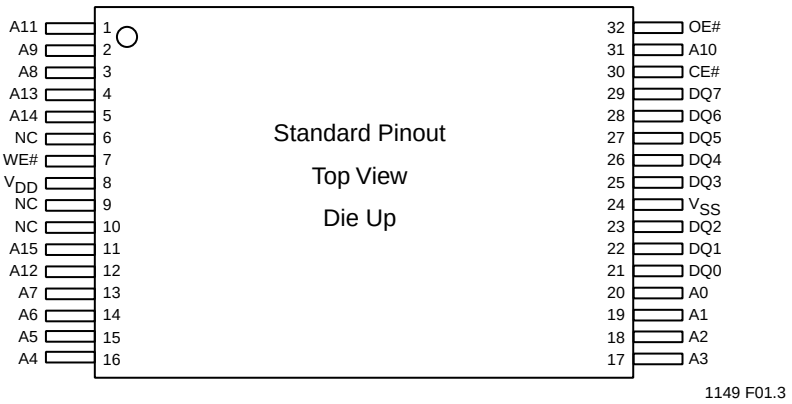


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)

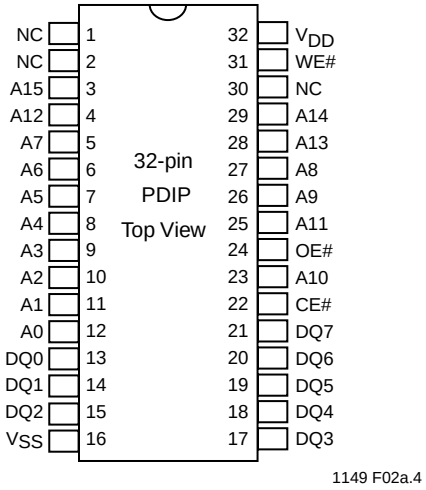


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{12} address lines will select the sector.
DQ_7-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide 4.5-5.5V supply
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

T2.4 1149

1. A_{MS} = Most significant address
   A_{MS} = A_{15} for SST39SF512 and A_{16} for SST39SF010

TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X[1]	Sector address, XXH for Chip-Erase
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
	X	X	V_{IH}	High Z/ D_{OUT}	X
Product Identification					
Software Mode	V_{IL}	V_{IL}	V_{IH}		See Table 4

T3.4 1149

1. X can be V_{IL} or V_{IH}, but no other value.

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte-Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[2]	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_X[3]	30H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry[4,5]	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit[6]	XXH	F0H										
Software ID Exit[6]	5555H	AAH	2AAAH	55H	5555H	F0H						

T4.3 1149

1. Address format A_{14}-A_0 (Hex), Address A_{15} can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
2. BA = Program Byte address
3. SA_X for Sector-Erase; uses A_{MS}-A_{12} address lines
   A_{MS} = Most significant address
   A_{MS} = A_{15} for SST39SF512
4. The device does not remain in Software Product ID mode if powered down.
5. With A_{MS}-A_1 = 0; SST Manufacturer's ID = BFH, is read with A_0 = 0,
   SST39SF512 Device ID = B4H, is read with A_0 = 1
6. Both Software ID Exit operations are equivalent

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Voltage on A_9 Pin to Ground Potential . . . . . -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hold Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 100 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	4.5-5.5V
Industrial	-40°C to +85°C	4.5-5.5V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . C_L = 30 pF for 70 ns
Output Load . . . . . C_L = 100 pF for 90 ns
See Figures 13 and 14

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 4.5-5.5V[1]

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input=V_{ILT}/V_{IHT}, at f=1/T_{RC} Min V_{DD}=V_{DD} Max
	Read[2]		30	mA	CE#=V_{IL}, OE#=WE#=V_{IH}, all I/Os open
	Program and Erase		50	mA	CE#=WE#=V_{IL}, OE#=V_{IH}
I_{SB1}	Standby V_{DD} Current (TTL input)		3	µA	CE#=V_{IH}, V_{DD}=V_{DD} Max
I_{SB2}	Standby V_{DD} Current (CMOS input)		50	µA	CE#=V_{DD} -0.3V, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	2.0		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=2.1 mA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-400 µA, V_{DD}=V_{DD} Min

T5.6 1149

1. Typical conditions for the Active Current shown on the front data sheet page are average values at 25°C (room temperature), and V_{DD} = 5V for SF devices. Not 100% tested.
2. Values are for 70 ns conditions. See the *Multi-Purpose Flash Power Rating* application note for further information.

TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Program/Erase Operation	100	µs

T6.1 1149

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

T7.0 1149

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1,2]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T8.2 1149

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. N_{END} endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V_{DD} = 4.5-5.5V

Symbol	Parameter	SST39SF512-70		Units
		Min	Max	
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{CLZ}[1]	CE# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	CE# High to High-Z Output		25	ns
T_{OHZ}[1]	OE# High to High-Z Output		25	ns
T_{OH}[1]	Output Hold from Address Change	0		ns

T9.5 1149

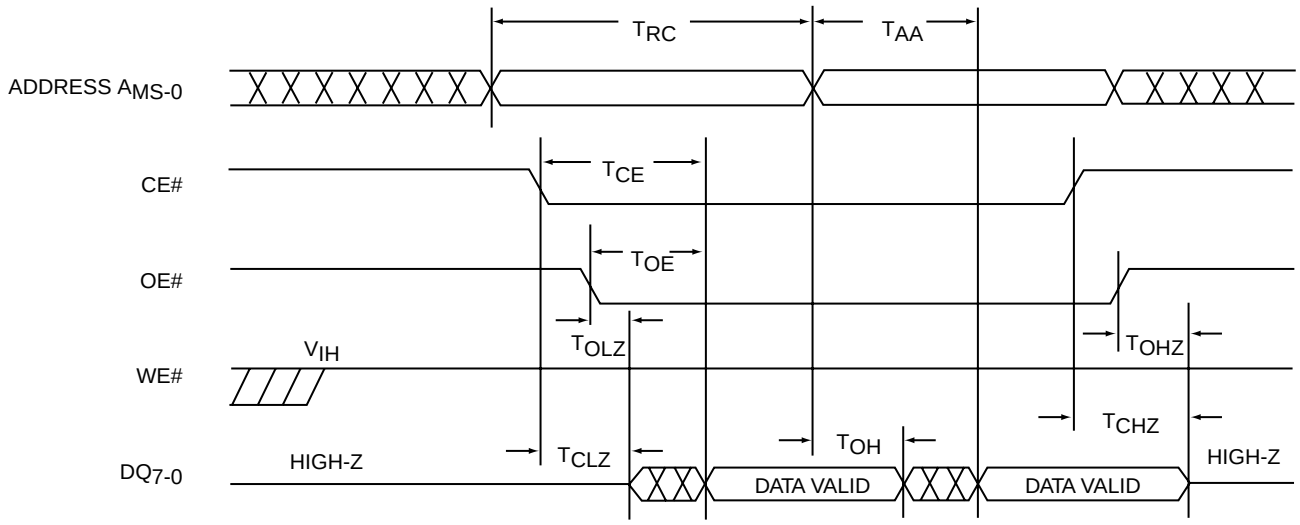
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Byte-Program Time		30	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		10	ms
T_{SCE}	Chip-Erase		20	ms

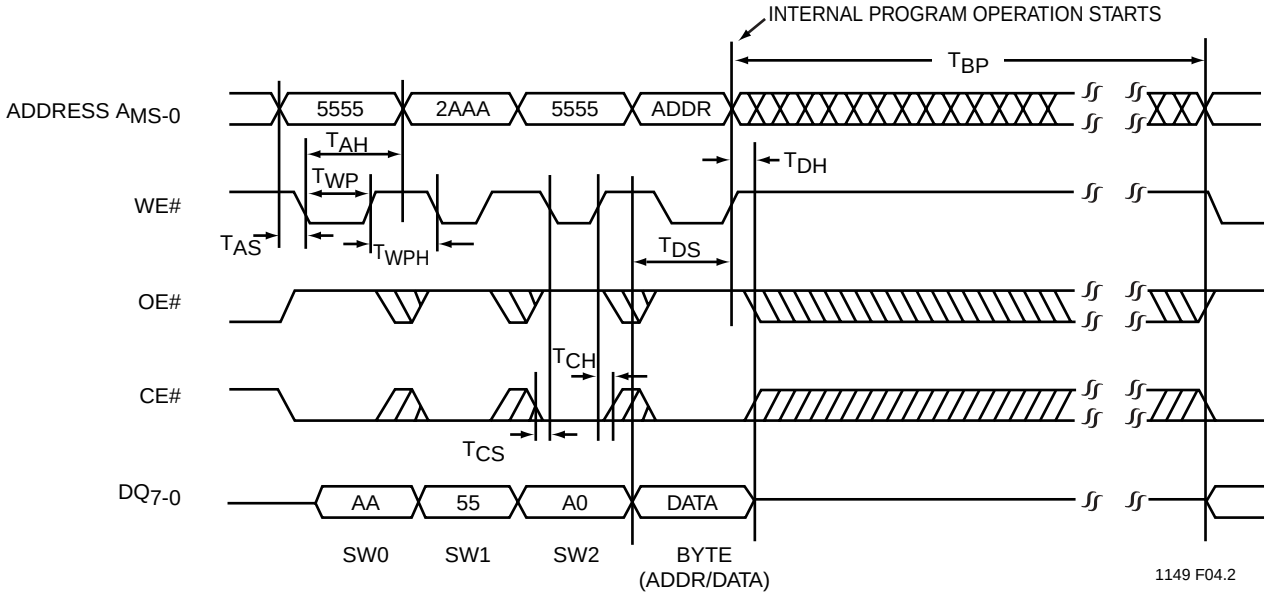
T10.1 1149

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



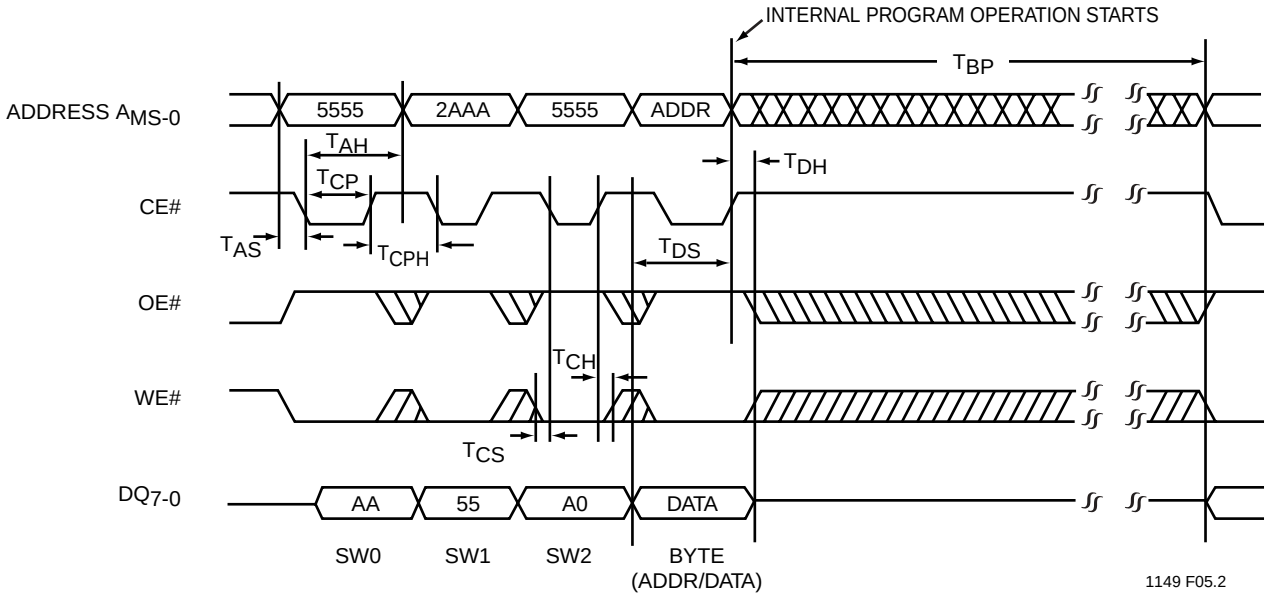
Note: A_{MS} = Most significant address
$A_{MS} = A_{15}$ for SST39SF512

FIGURE 4: READ CYCLE TIMING DIAGRAM



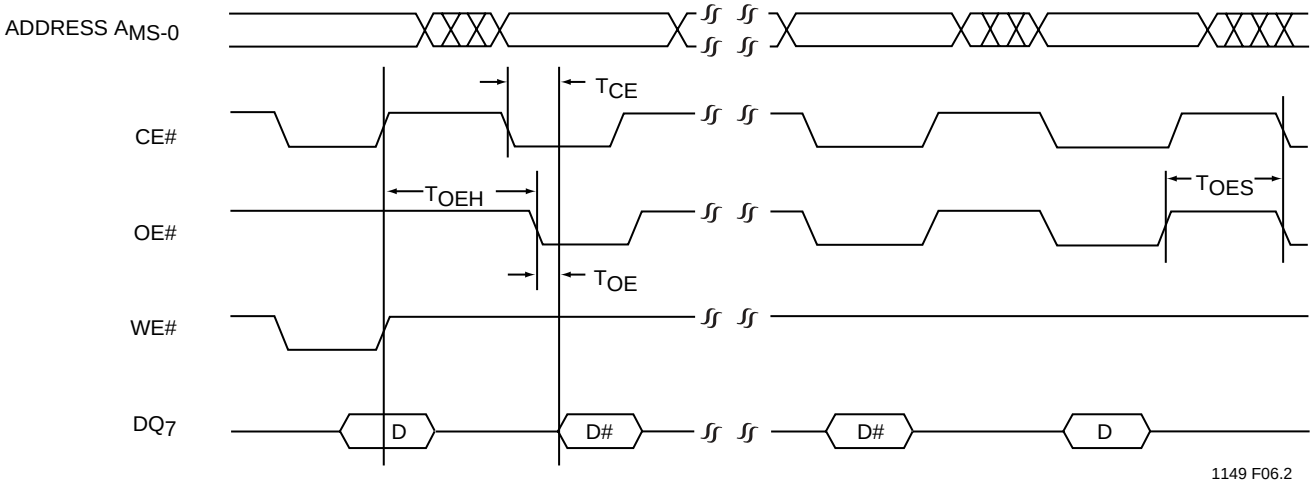
Note: A_{MS} = Most significant address
$A_{MS} = A_{15}$ for SST39SF512

FIGURE 5: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



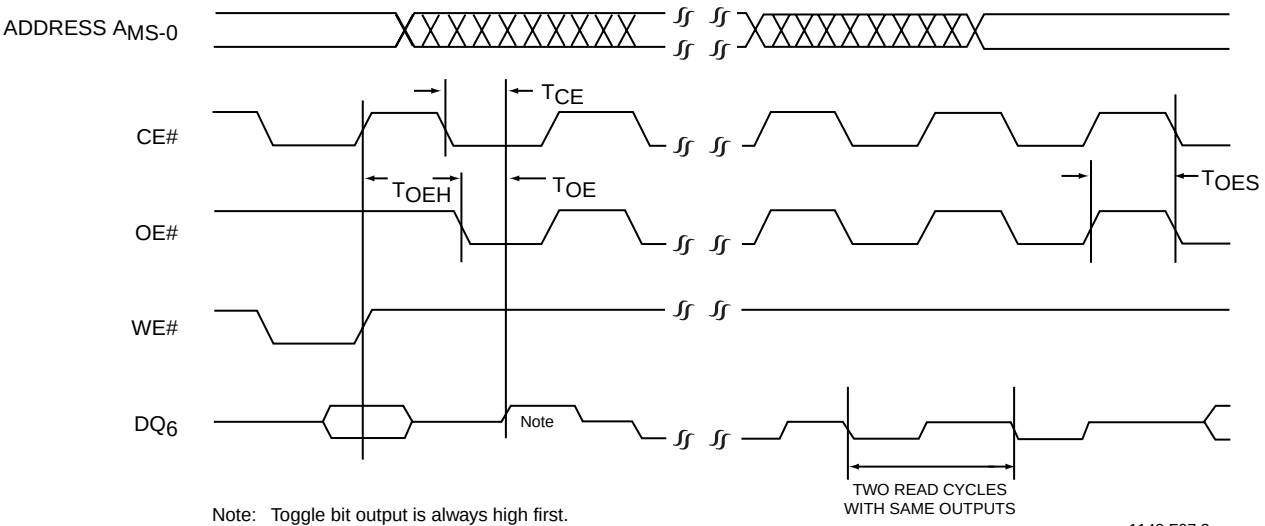
Note: A_{MS} = Most significant address
$A_{MS} = A_{15}$ for SST39SF512

FIGURE 6: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



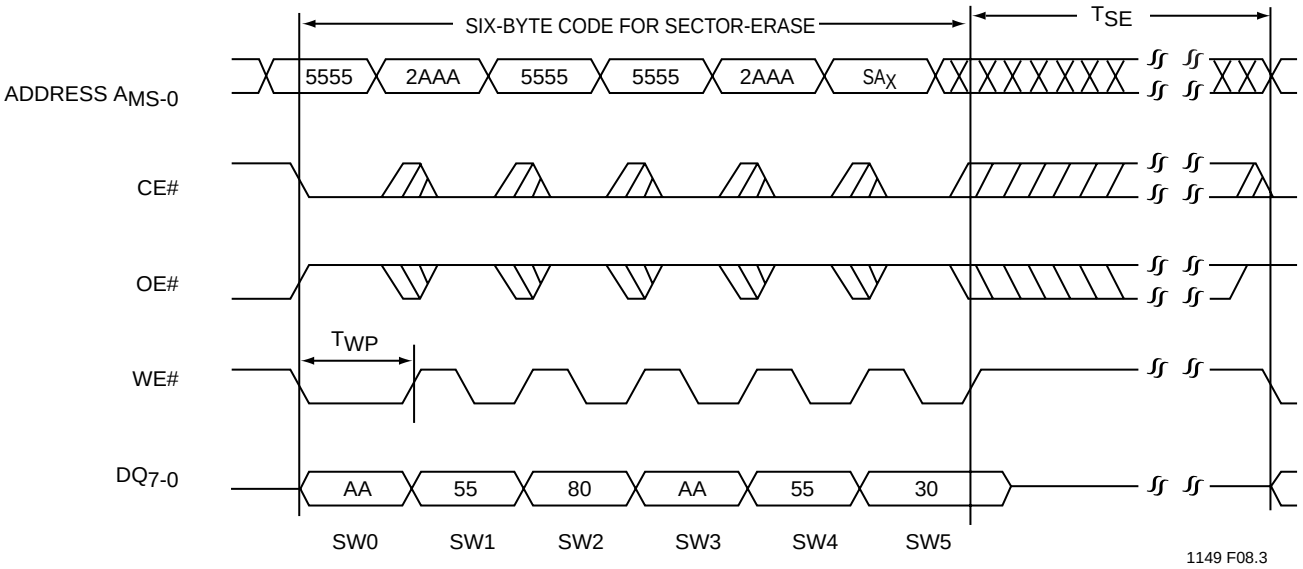
Note: A_{MS} = Most significant address
$A_{MS} = A_{15}$ for SST39SF512

FIGURE 7: DATA# POLLING TIMING DIAGRAM



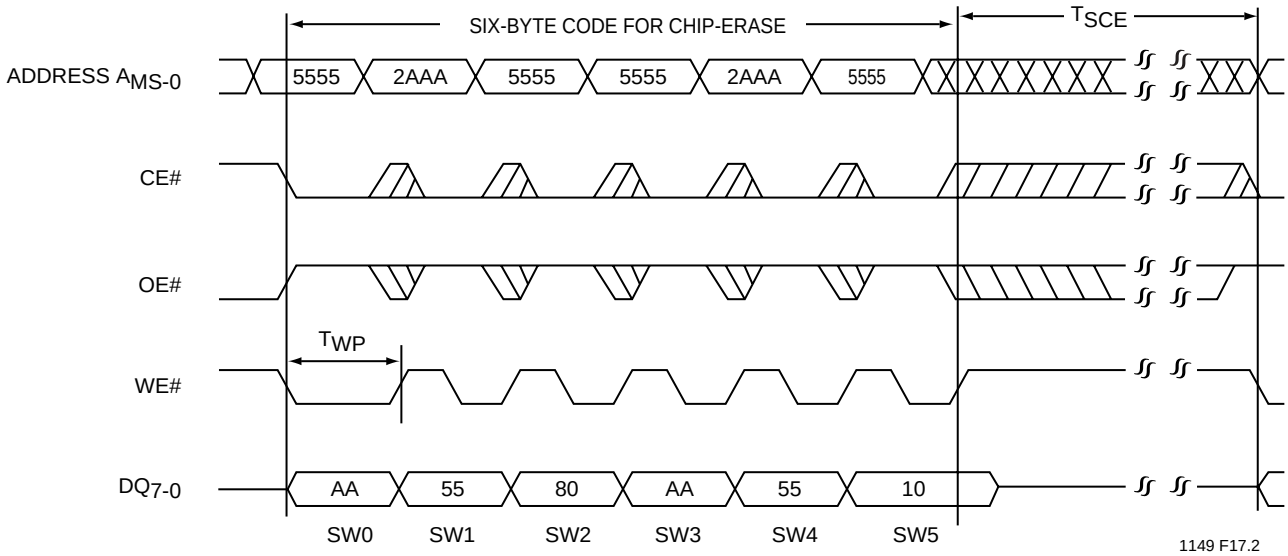
Note: Toggle bit output is always high first.
A_{MS} = Most significant address
A_{MS} = A_{15} for SST39SF512

FIGURE 8: TOGGLE BIT TIMING DIAGRAM



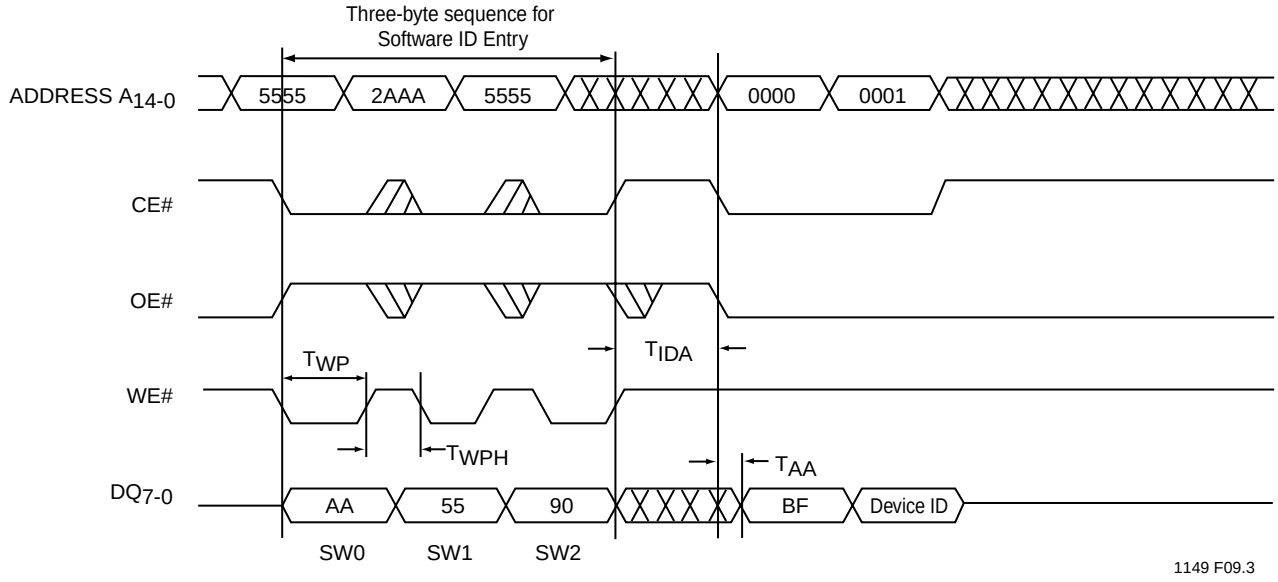
Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address
A_{MS} = Most significant address
A_{MS} = A_{15} for SST39SF512

FIGURE 9: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchageable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address
A_{MS} = Most significant address
A_{MS} = A_{15} for SST39SF512

FIGURE 10: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



Device ID = B4H for SST39SF512

FIGURE 11: SOFTWARE ID ENTRY AND READ

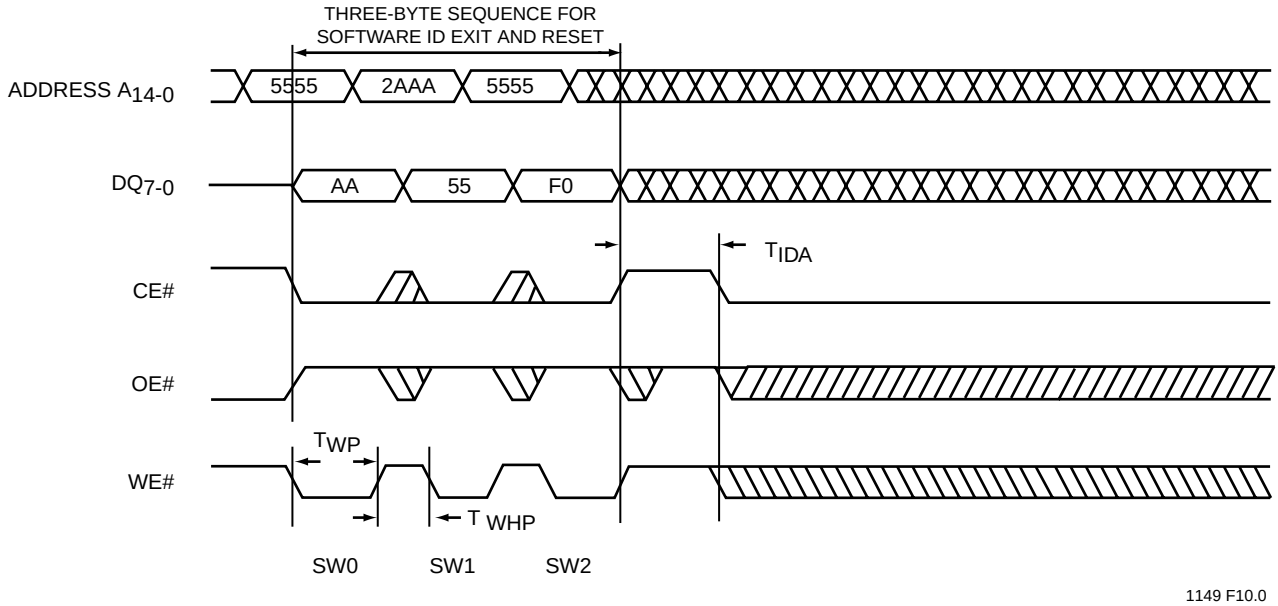
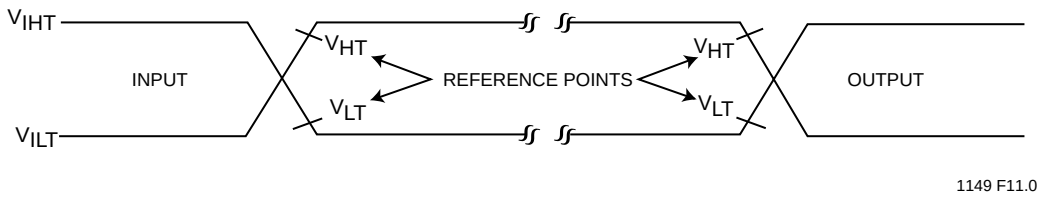


FIGURE 12: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (2.4V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} (2.0 V) and V_{LT} (0.8 V). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS

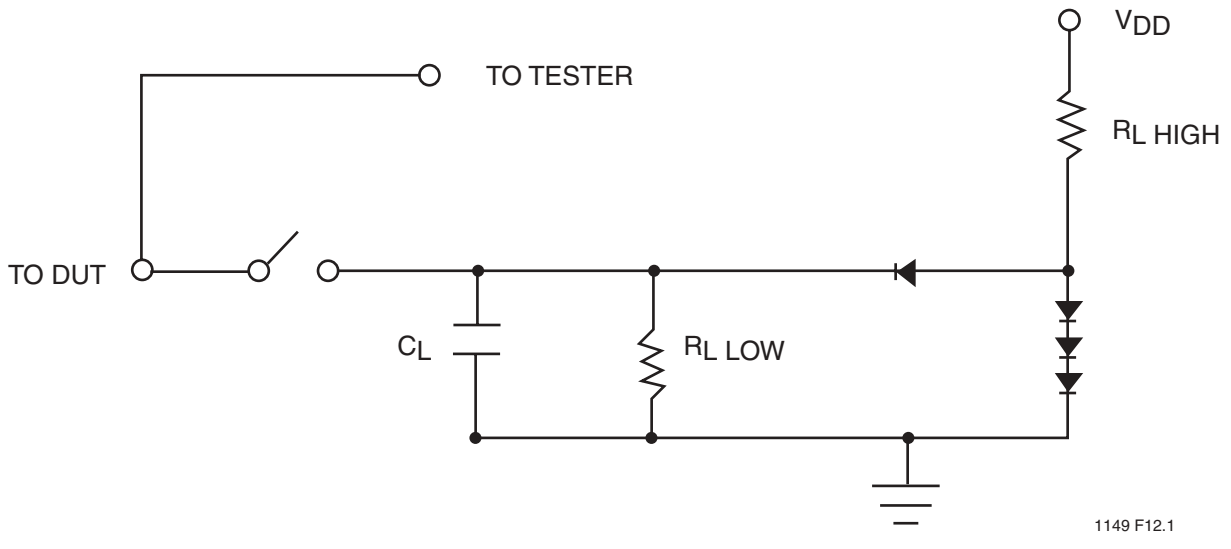


FIGURE 14: A TEST LOAD EXAMPLE

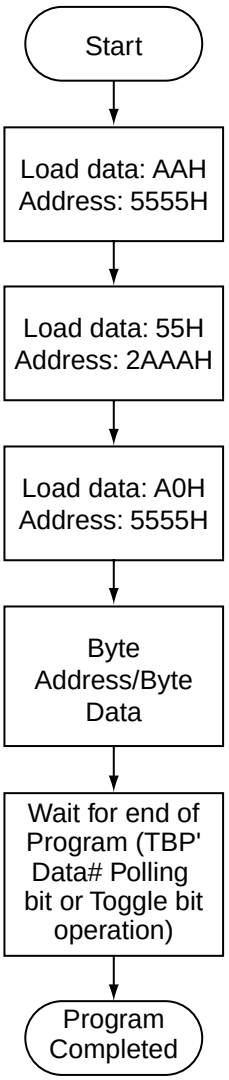


FIGURE 15: BYTE-PROGRAM ALGORITHM

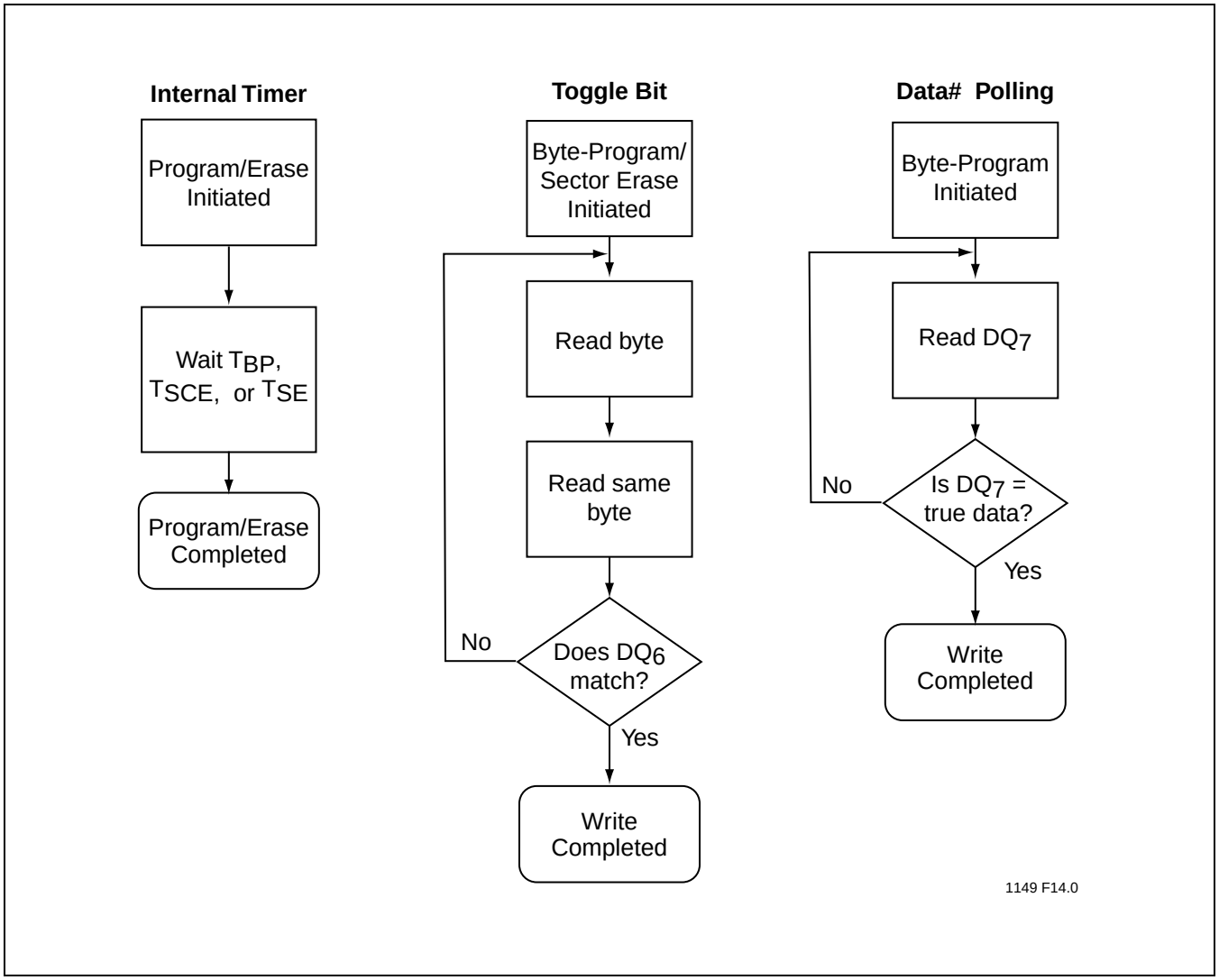


FIGURE 16: WAIT OPTIONS

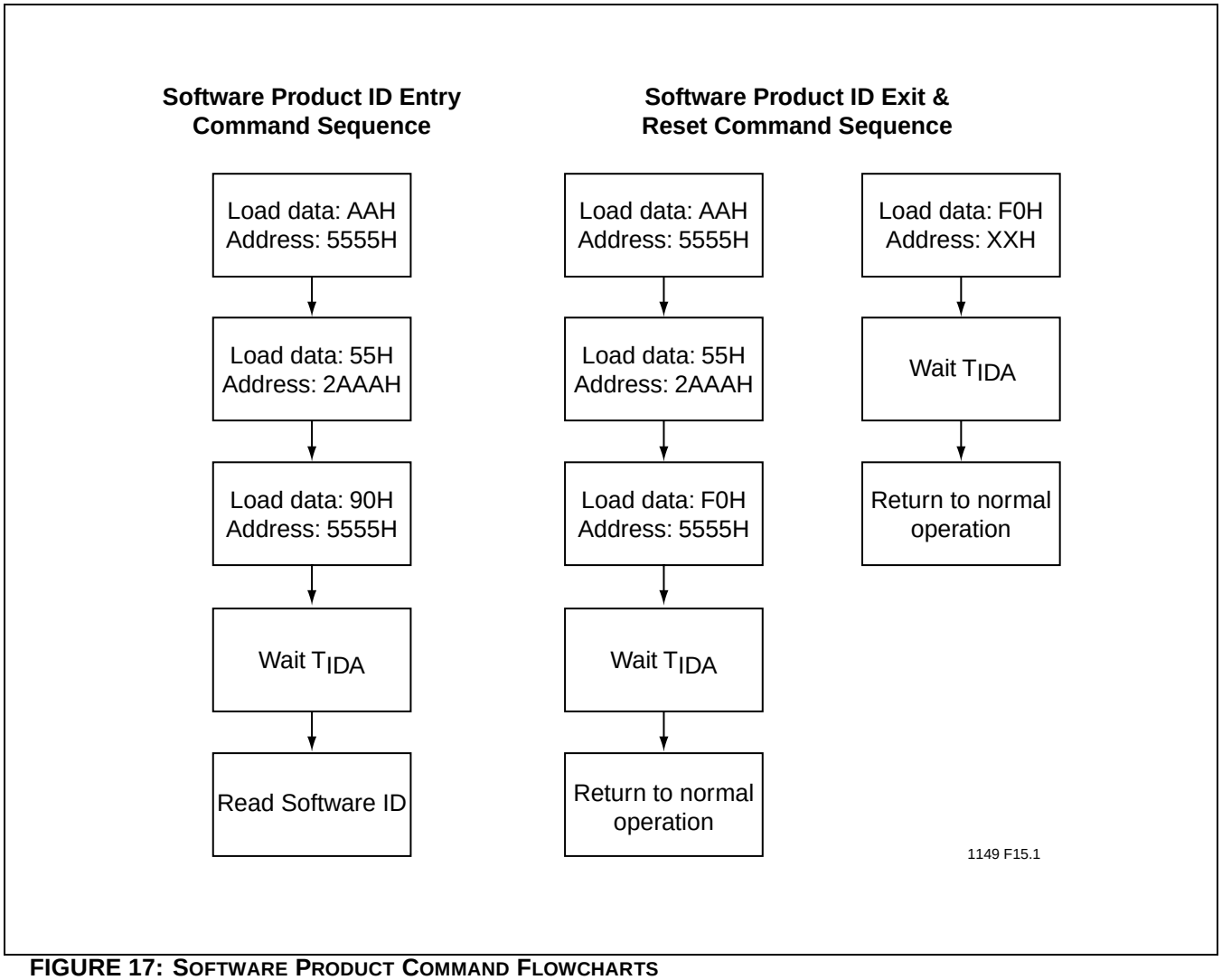


FIGURE 17: SOFTWARE PRODUCT COMMAND FLOWCHARTS

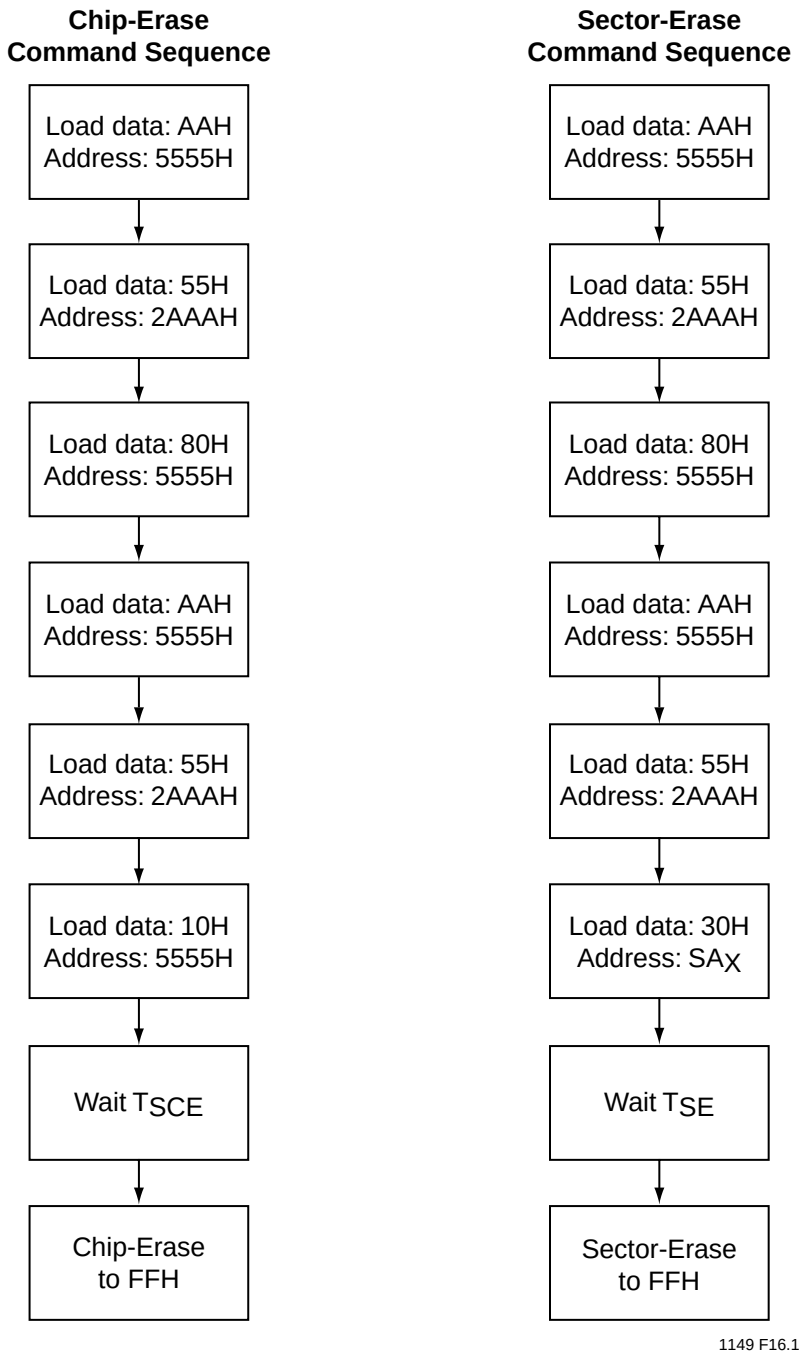
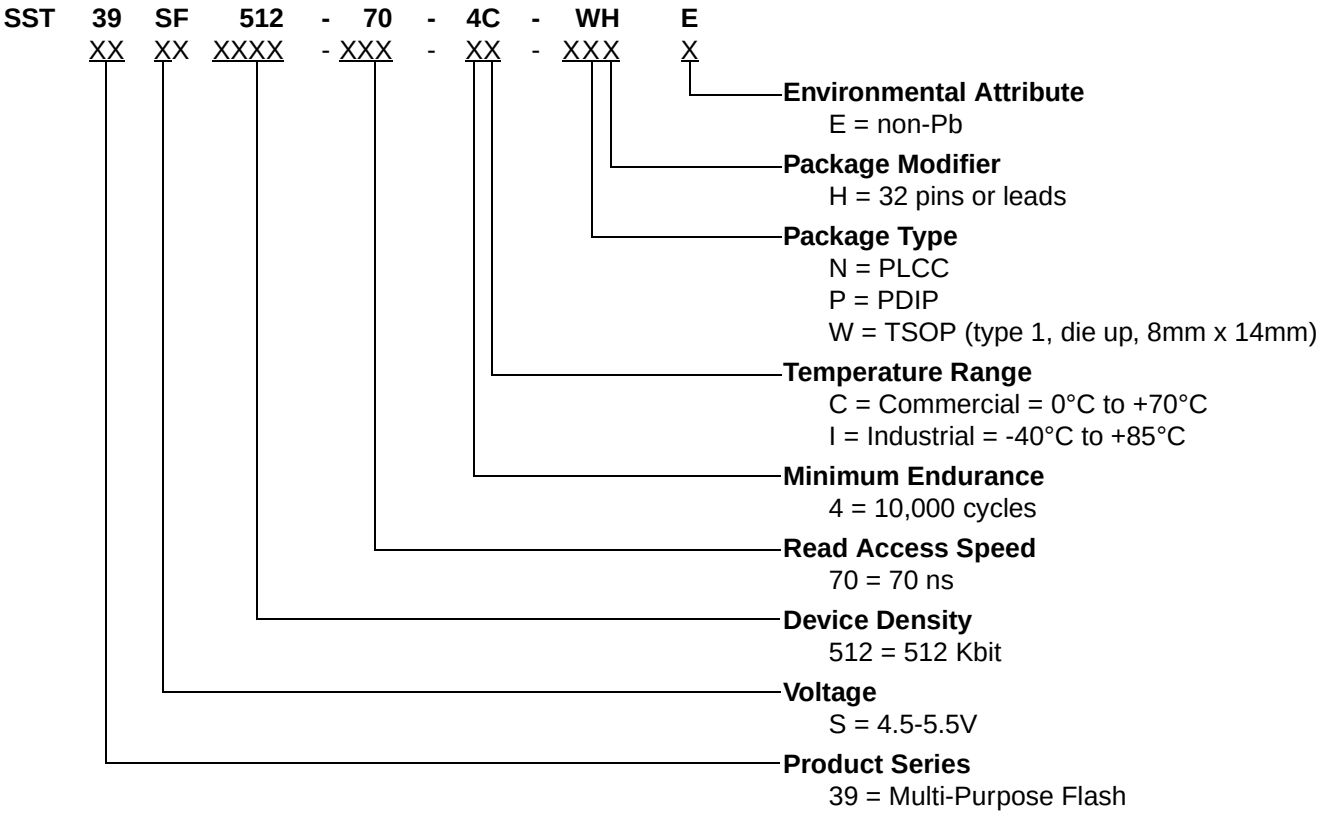


FIGURE 18: ERASE COMMAND SEQUENCE

PRODUCT ORDERING INFORMATION

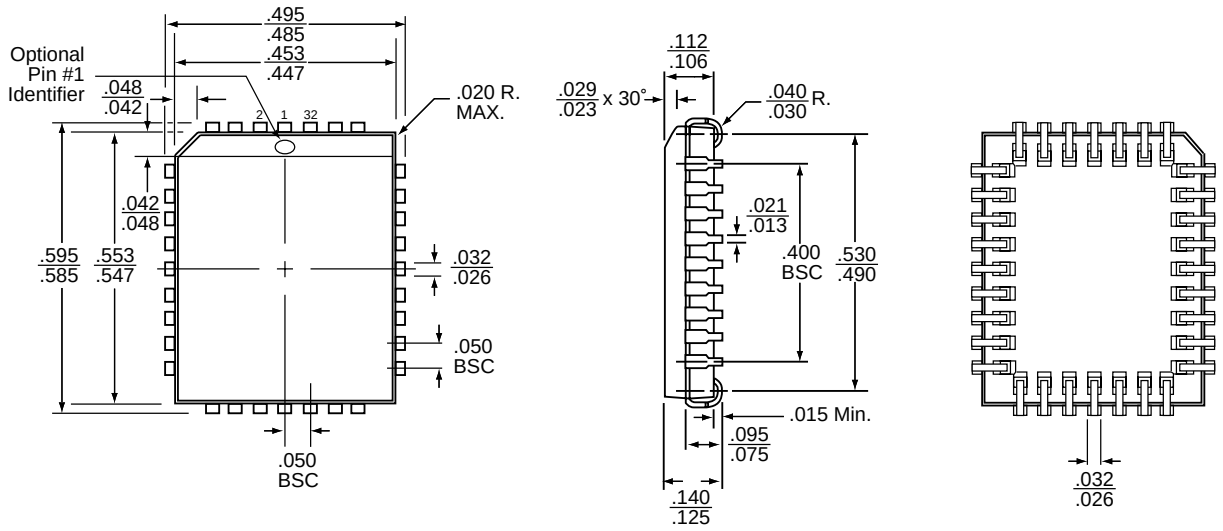


Valid combinations for SST39SF512

SST39SF512-70-4C-NH	SST39SF512-70-4C-WH	SST39SF512-70-4C-PH
SST39SF512-70-4C-NHE	SST39SF512-70-4C-WHE	
SST39SF512-70-4I-NH	SST39SF512-70-4I-WH	
SST39SF512-70-4I-NHE	SST39SF512-70-4I-WHE	

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

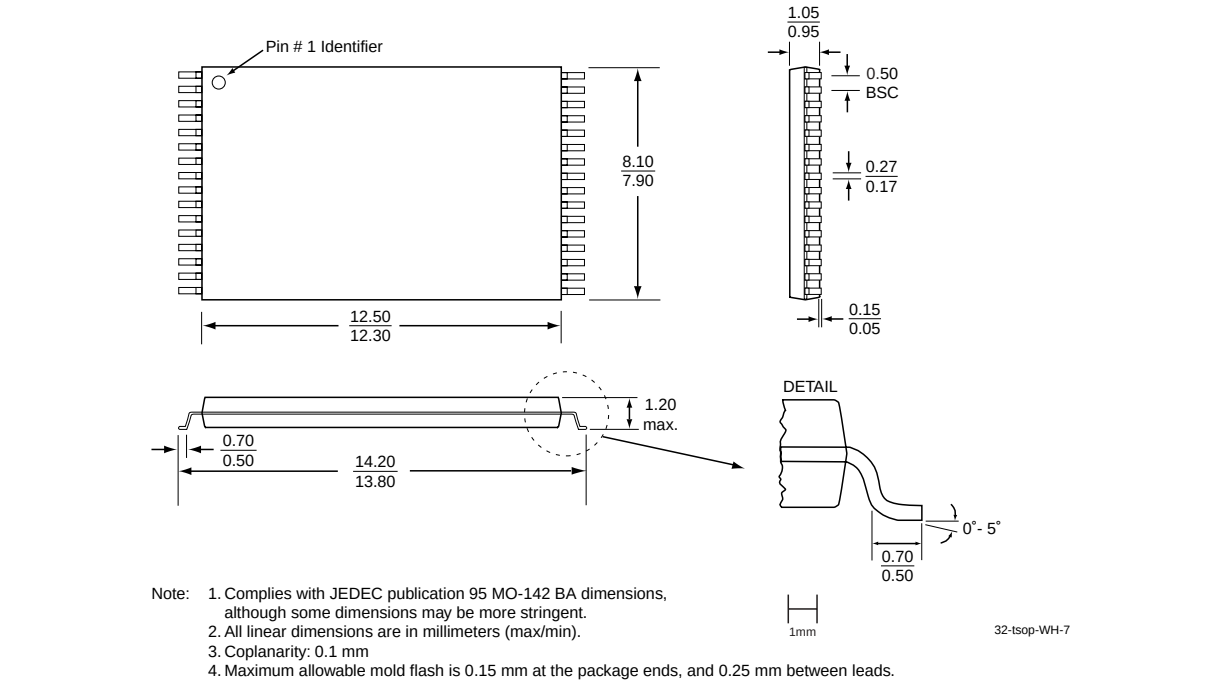
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32-plcc-NH-3

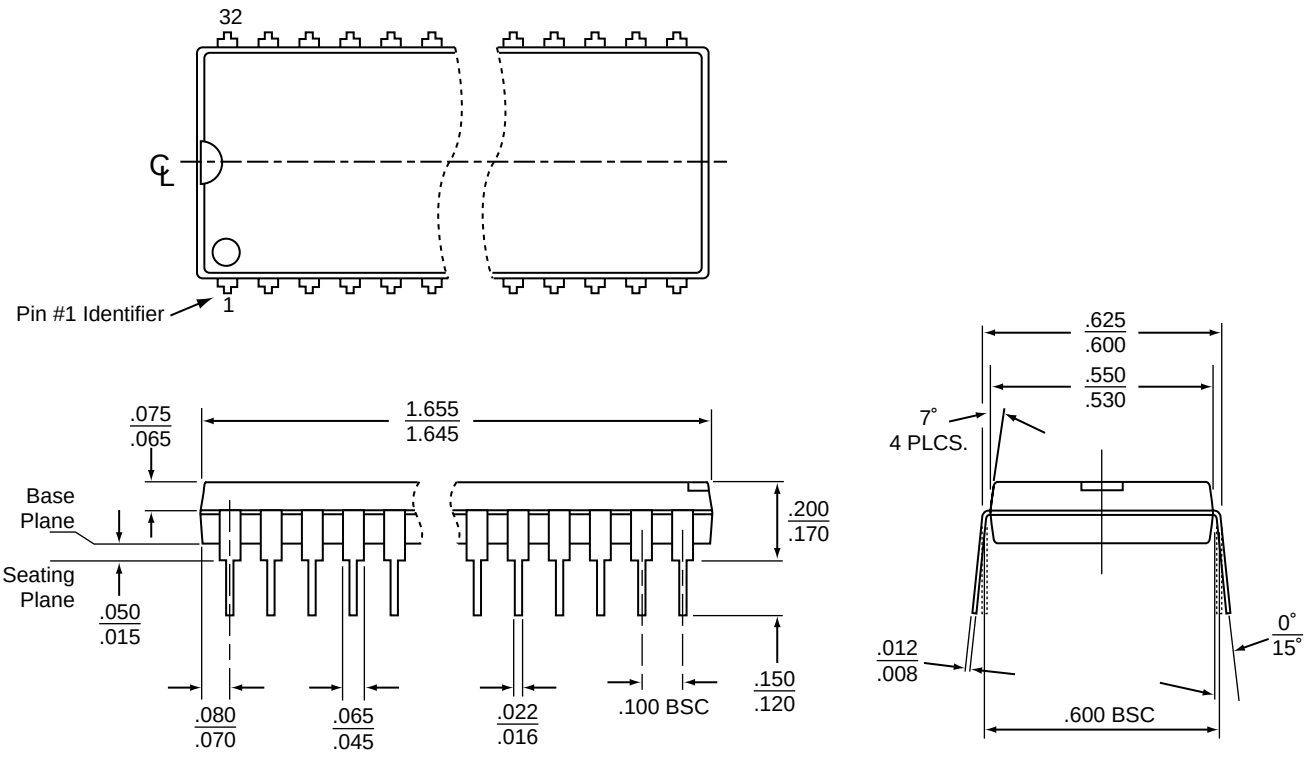
32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-tsop-WH-7

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32-pdip-PH-3

32-PIN PLASTIC DUAL IN-LINE PINS (PDIP)
SST PACKAGE CODE: PH

TABLE 11: REVISION HISTORY

Number	Description	Date
03	• 2002 Data Book	Apr 2002
04	• Removed 1 Mbit part • Added footnote for MPF power usage and Typical conditions to Table 5 on page 8 • Clarified the Test Conditions for Power Supply Current and Read parameters in Table 5 • Part number changes - see page 20 for additional information • 90 ns parts are no longer offered • Clarifed I_{DD} Write to be Program and Erase in Table 5 on page 8	Mar 2003
05	• 2004 Data Book • Added non-Pb MPNs and removed footnote (See page 20)	Nov 2003